|  |  |
| --- | --- |
| Alu operation (F0) (5 bit) | code |
| 00000 | A and b |
| 00001 | A or b |
| 00010 | A xnor b |
| 00011 | Not A |
| 00100 | Shift right A |
| 00101 | Rotate right A |
| 00110 | Rotate right with carry A |
| 00111 | Arithmetic shift right A |
| 01000 | Shift left |
| 01001 | Rotate left |
| 01010 | Rotate left with carry |
| 01011 | Transfer A |
| 01100 | Transfer B |
| 01101 | Clear f=0 |
| 10000 | A+B |
| 10001 | A+B+carry |
| 10010 | A-B |
| 10011 | a-b-carry |
| 10100 | a-1 |

|  |  |
| --- | --- |
| Out A (F1) (4 bits) | Register outing on A |
| 0000 | Rn src |
| 0001 | Rn dst |
| 0010 | R6(PC) |
| 0011 | R7(SP) |
| 0100 | MDR |
| 0101 | Temp1 |
| 0110 | Temp2 |
| 0111 | flag |
| 1000 | No operation |

|  |  |
| --- | --- |
| Out B (F2) (4 bits) | Register outing on B |
| 0000 | Rn src |
| 0001 | Rn dst |
| 0010 | R7(SP) |
| 0011 | MDR |
| 0100 | Temp1 |
| 0101 | Temp2 |
| 0110 | IR-----address filed of IR (:) |
| 0111 | flag |
| 1000 | No operation |

|  |  |
| --- | --- |
| Rn - Temp – IR in (F3)(4) | Register in from bus c |
| 0000 | Rn src |
| 0001 | Rn dst |
| 0010 | R6(pc) |
| 0011 | R7(sp) |
| 0100 | Temp1 |
| 0101 | Temp2 |
| 0110 | IR |
| 0111 | Inc pc |
| 1000 | No operation |

|  |  |
| --- | --- |
| MAR – MDR – Flag in (F4)(2) | Register in from bus c |
| 00 | MAR |
| 01 | MDr |
| 10 | Flag |
| 11 | No operation |

|  |  |
| --- | --- |
| Read - Write (F5)(2 bits ) | Read and write signal |
| 00 | Read |
| 01 | Write |
| 10 | No operation |

|  |  |
| --- | --- |
| Next Address (F6)(6 bits ) | At each micro instruction I have the next address field |
|  |  |
|  |  |
|  |  |

|  |  |
| --- | --- |
| Branch (F7)(3 bits ) |  |
| 000 | OR dst |
| 001 | OR indsrc |
| 010 | OR inddst |
| 011 | OR result |
| 100 | OR Operation |
| 101 | Branch check |
| 110 | No operation |